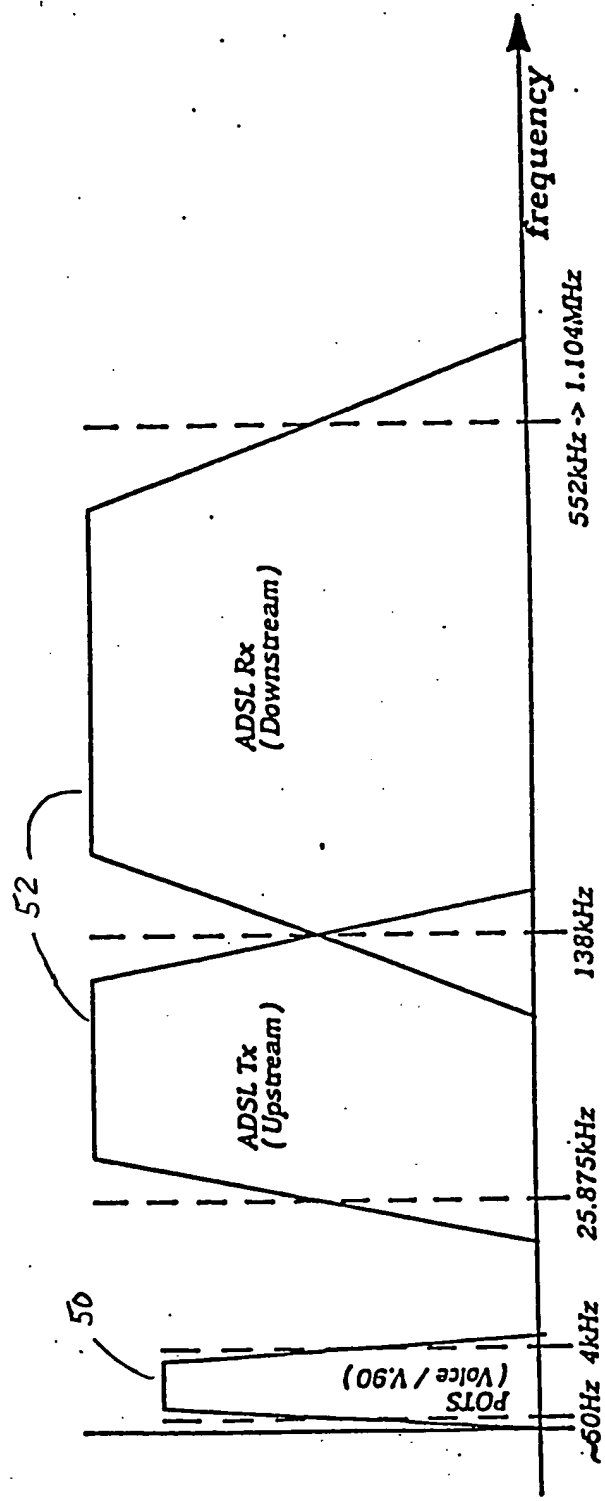


Fig 1  
Prior Art



Prior Art

Fig 2

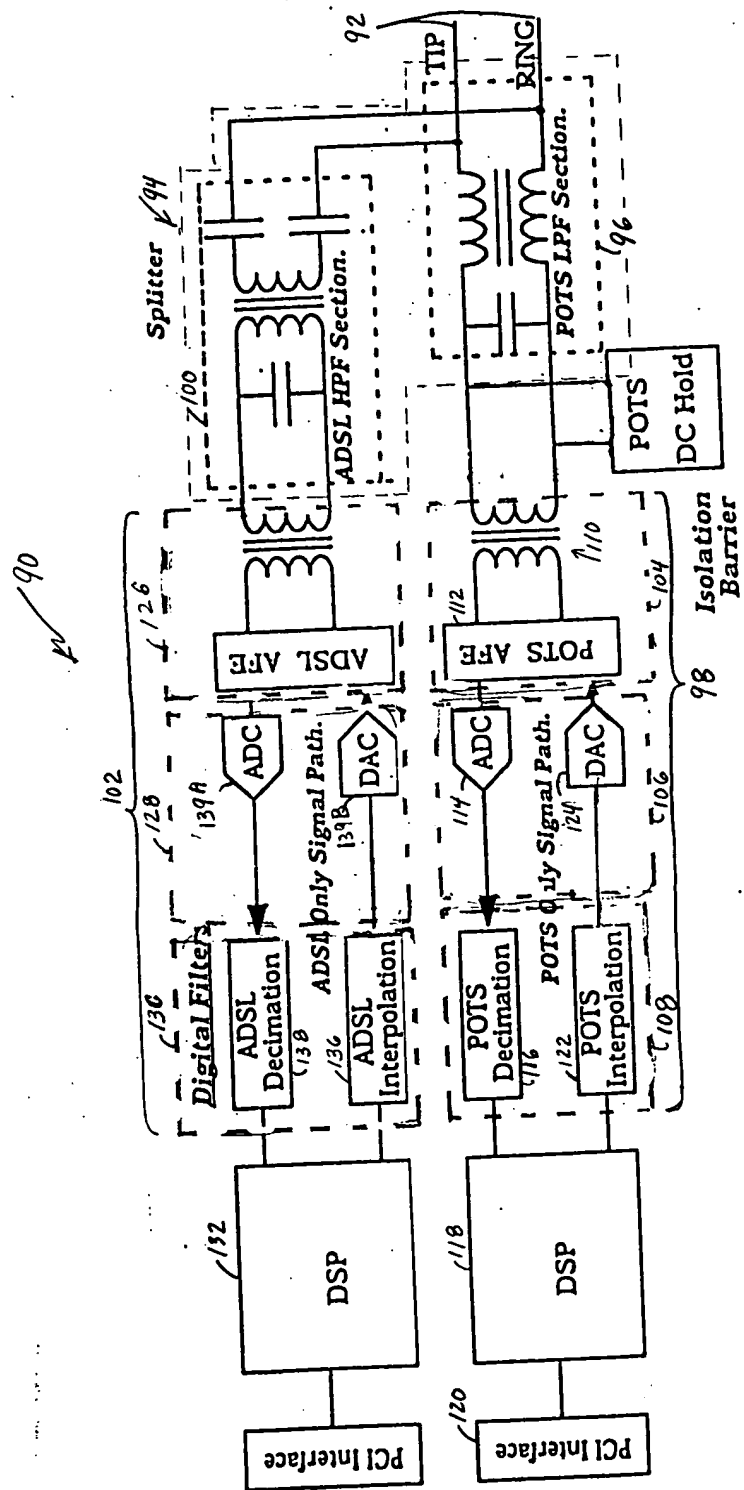


Fig. 3 Prior Art

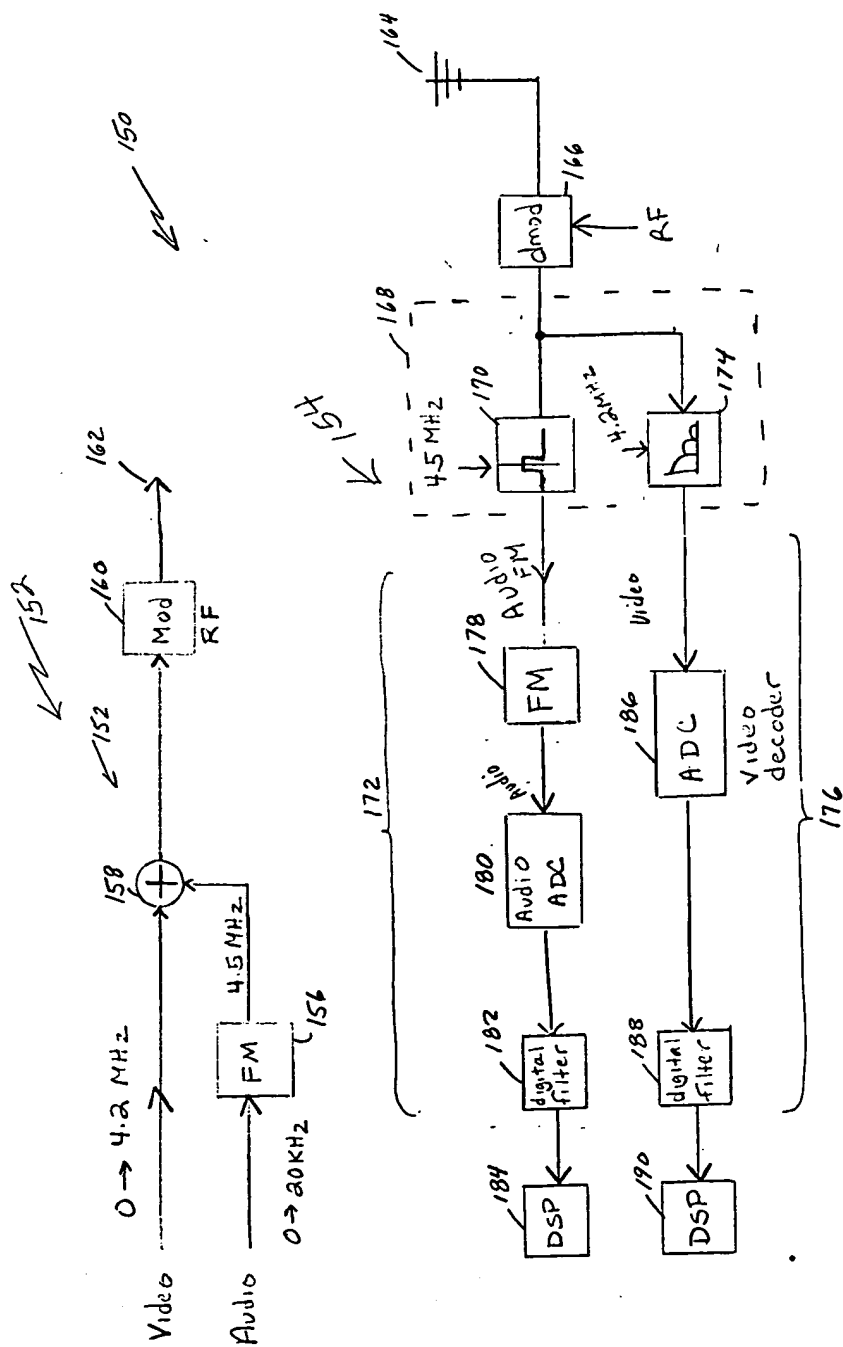


Fig 4 Prior Art

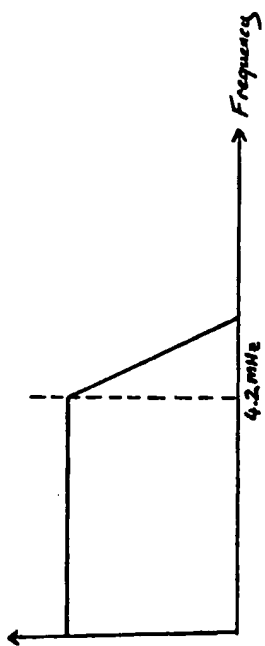


Fig. 5 Prior Art

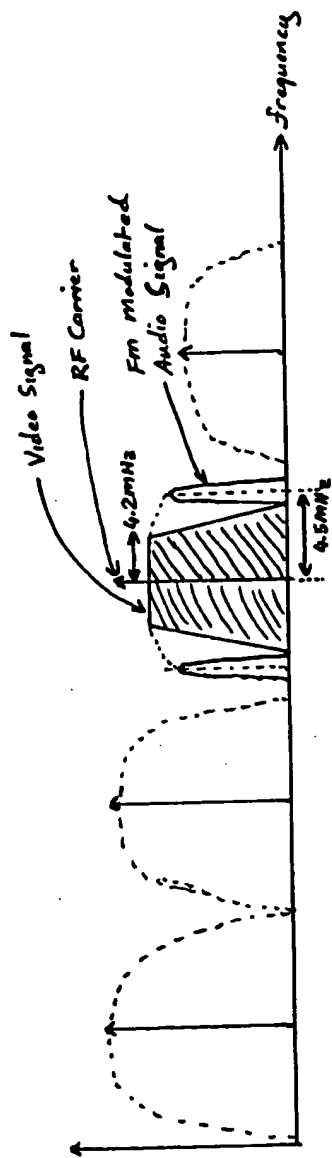


Fig. 6 Prior Art

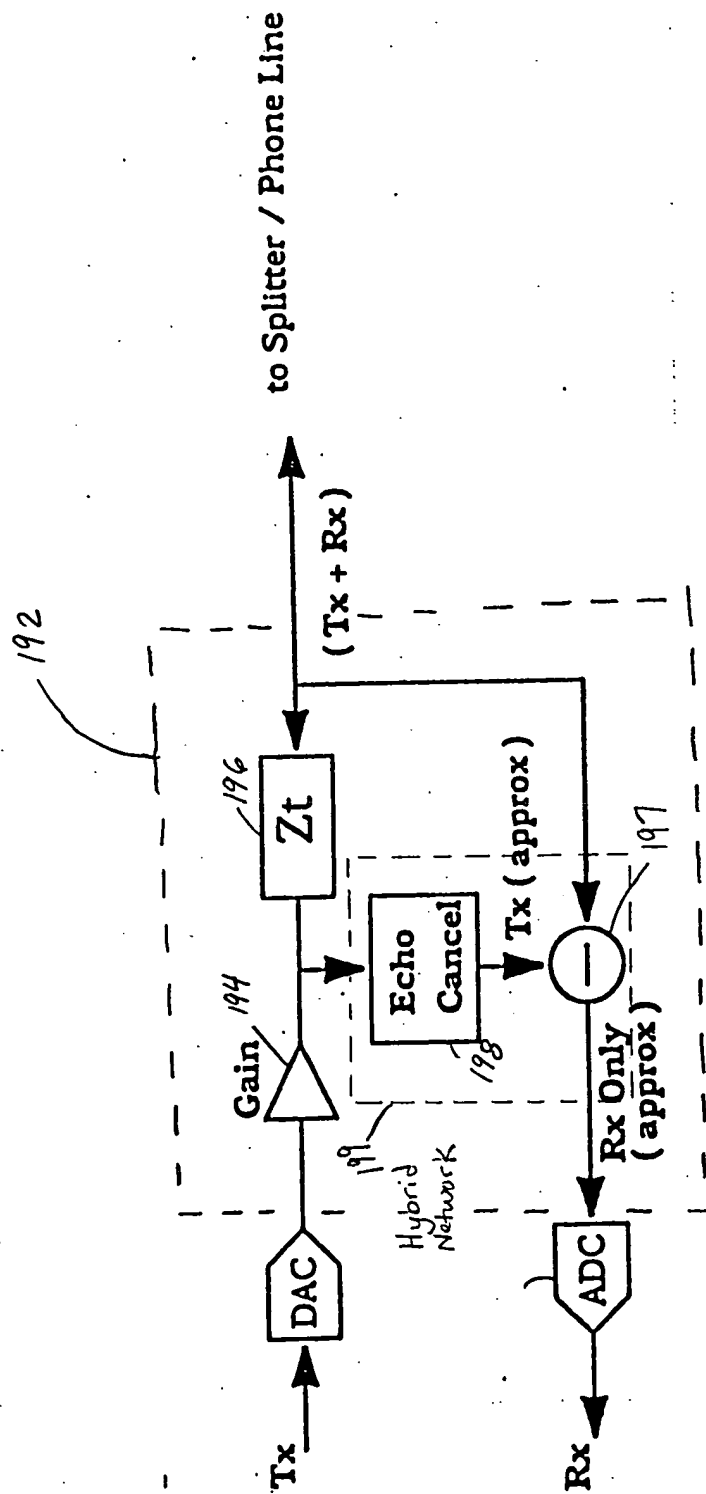


Fig. 7 Prior Art

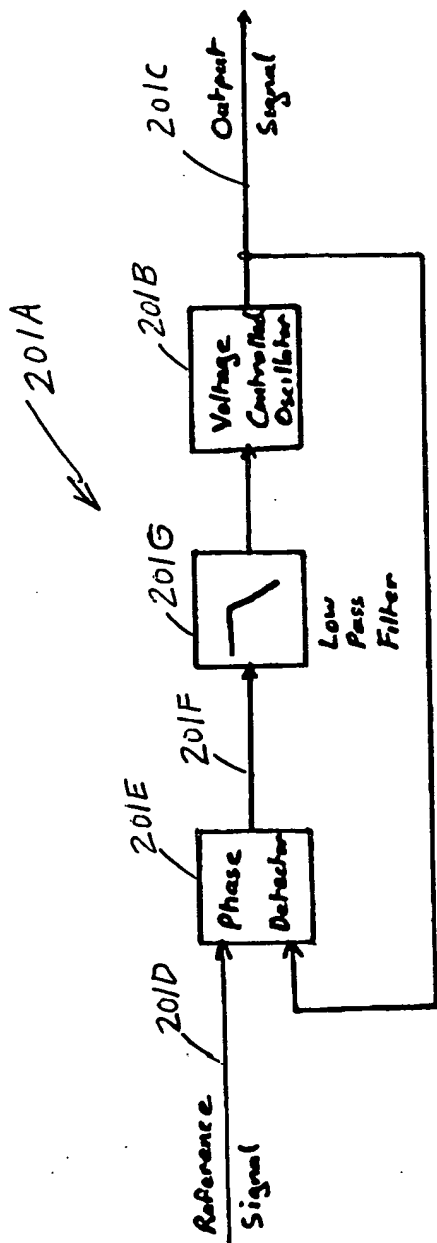


Fig 8 Prior Art

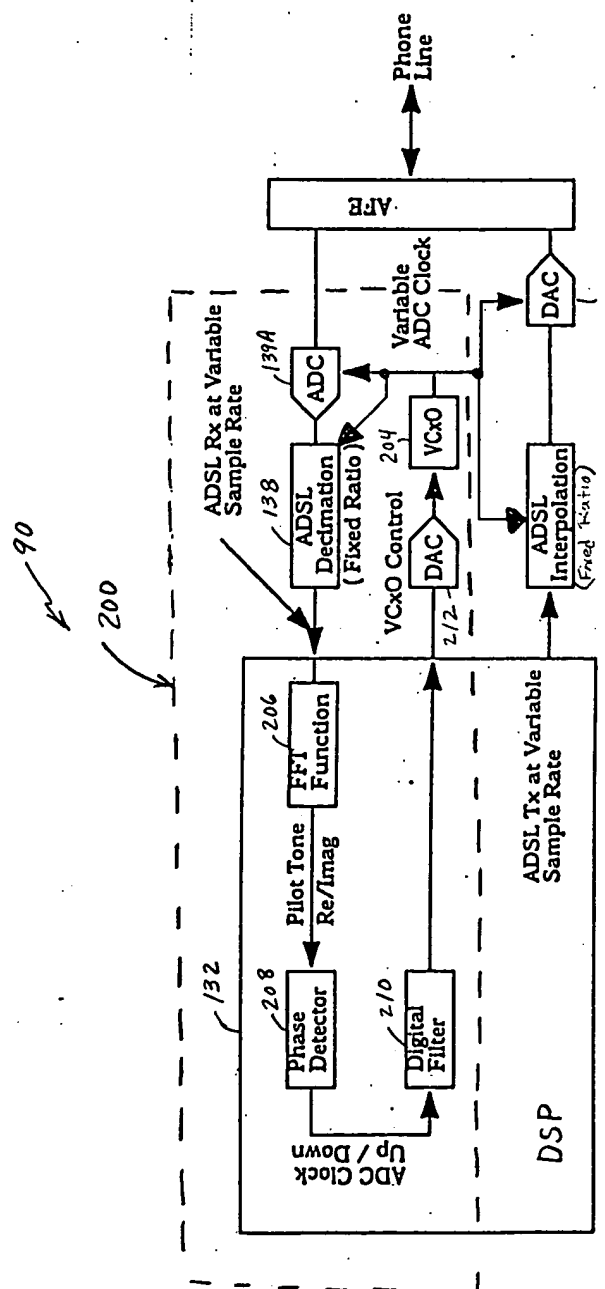


Fig. 9 Prior Art



FIG. 10 is a block diagram of a digital signal processing system 300.

300

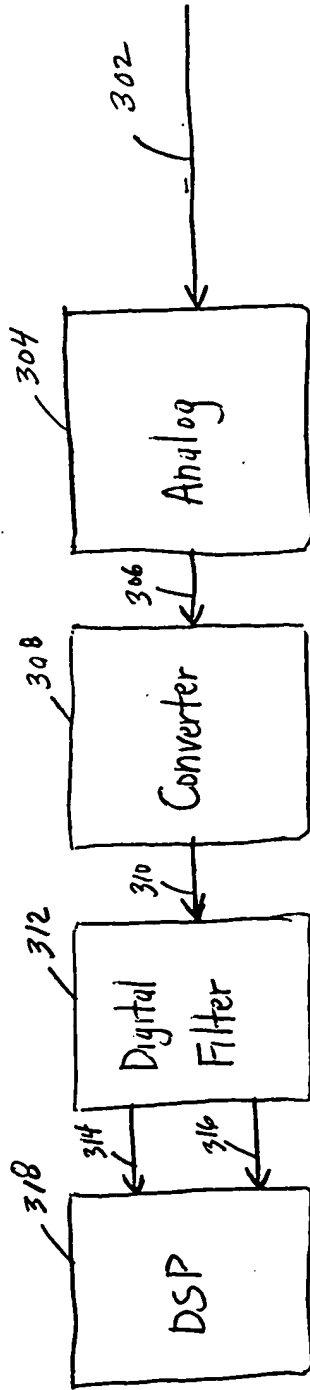


Fig. 10

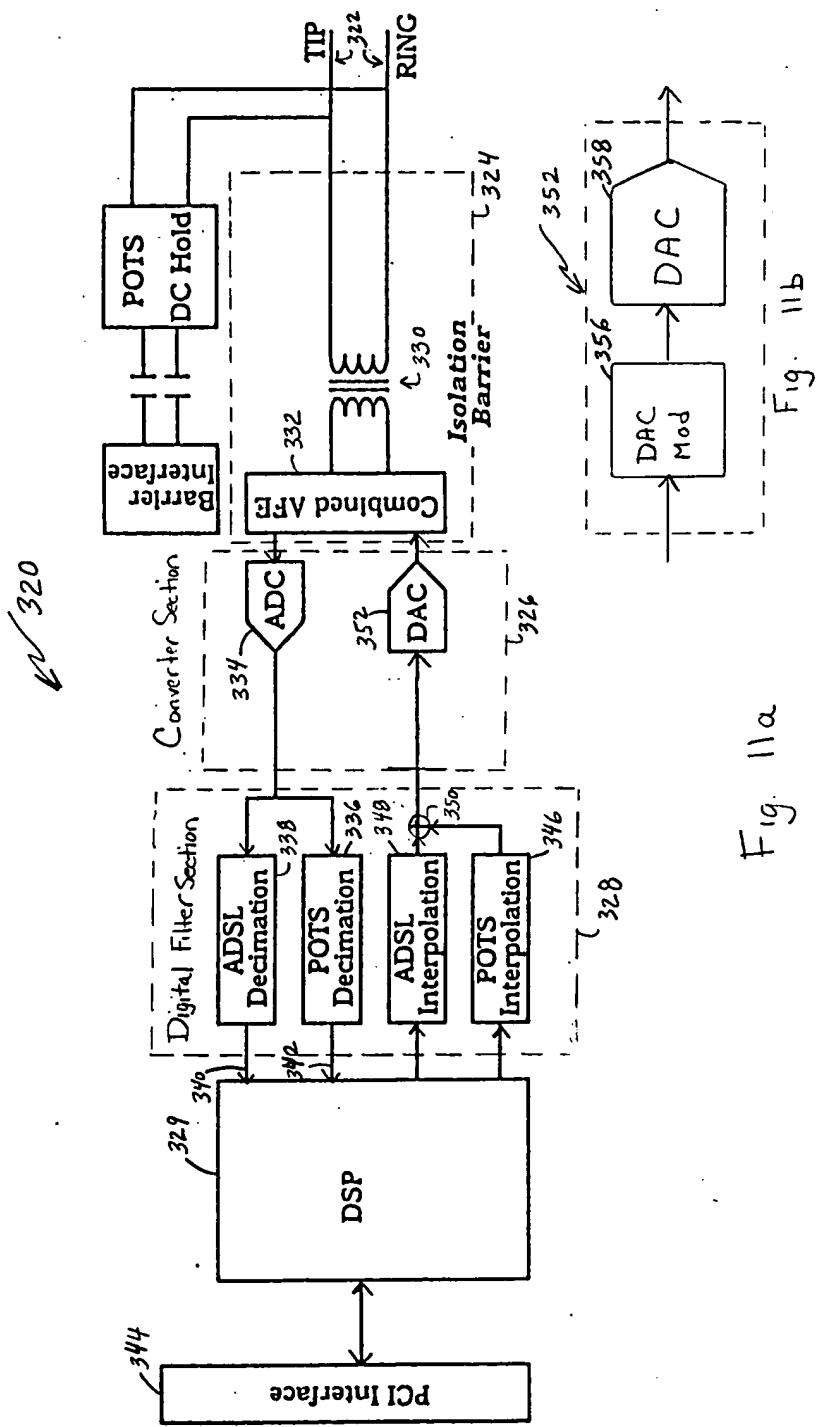


Fig. 11a

Fig. 11b

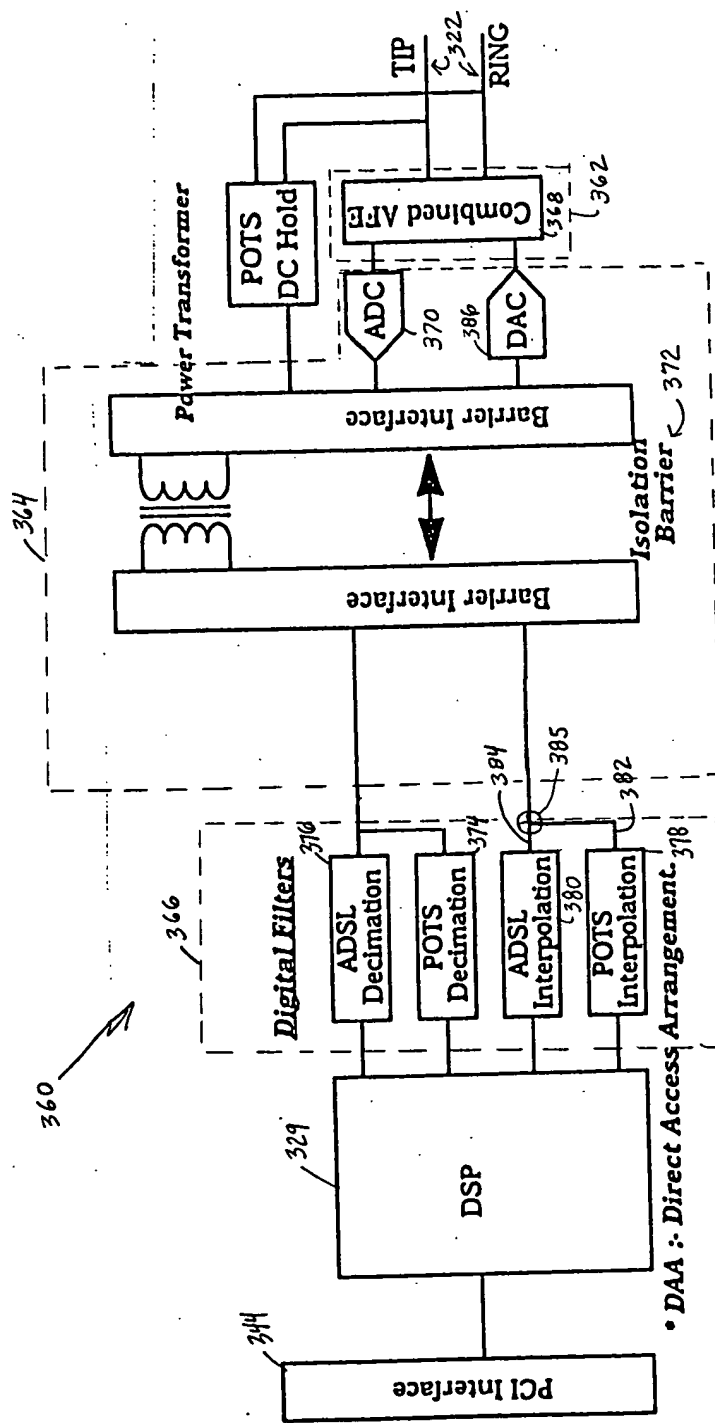


Fig. 12a

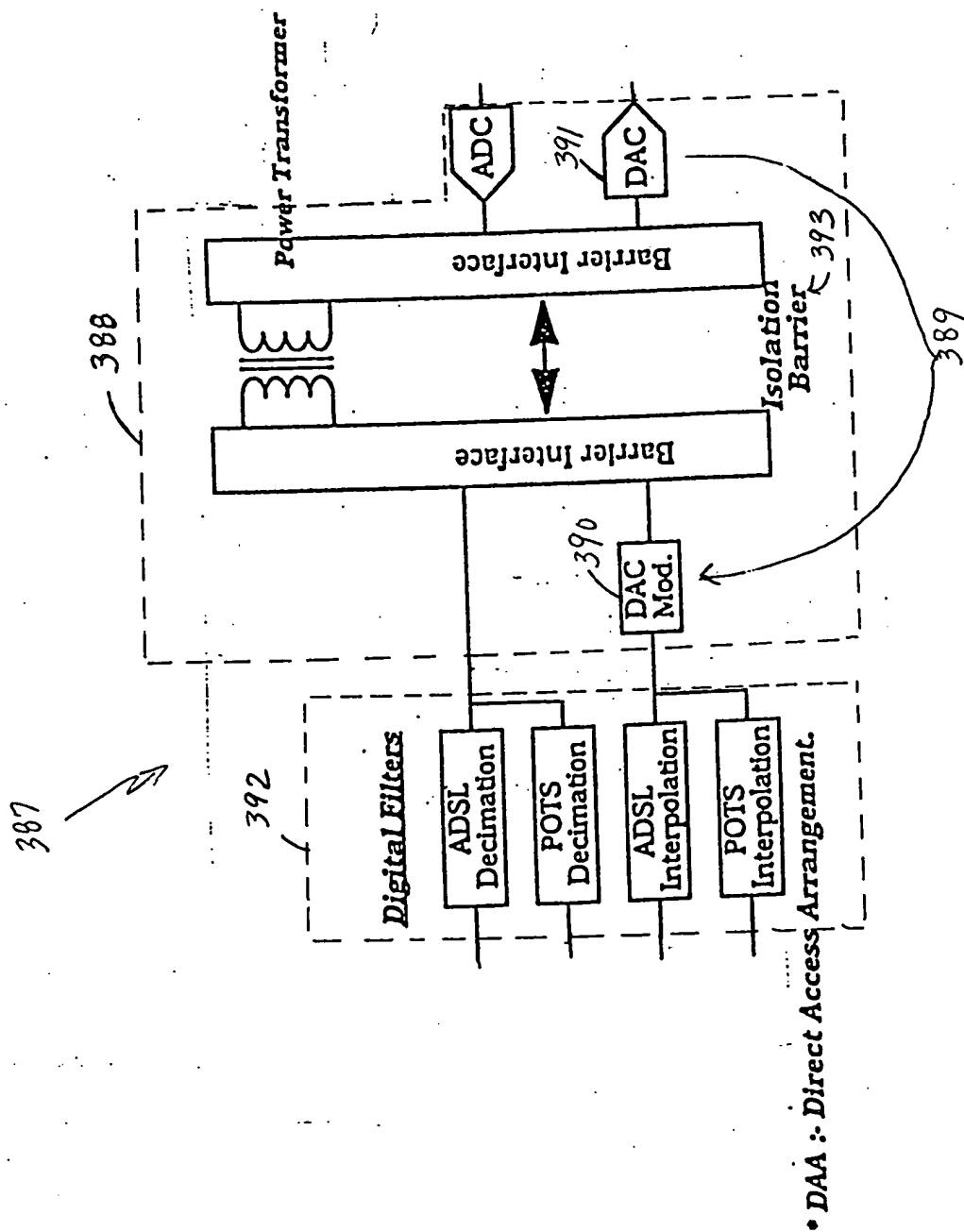


Fig. 12b

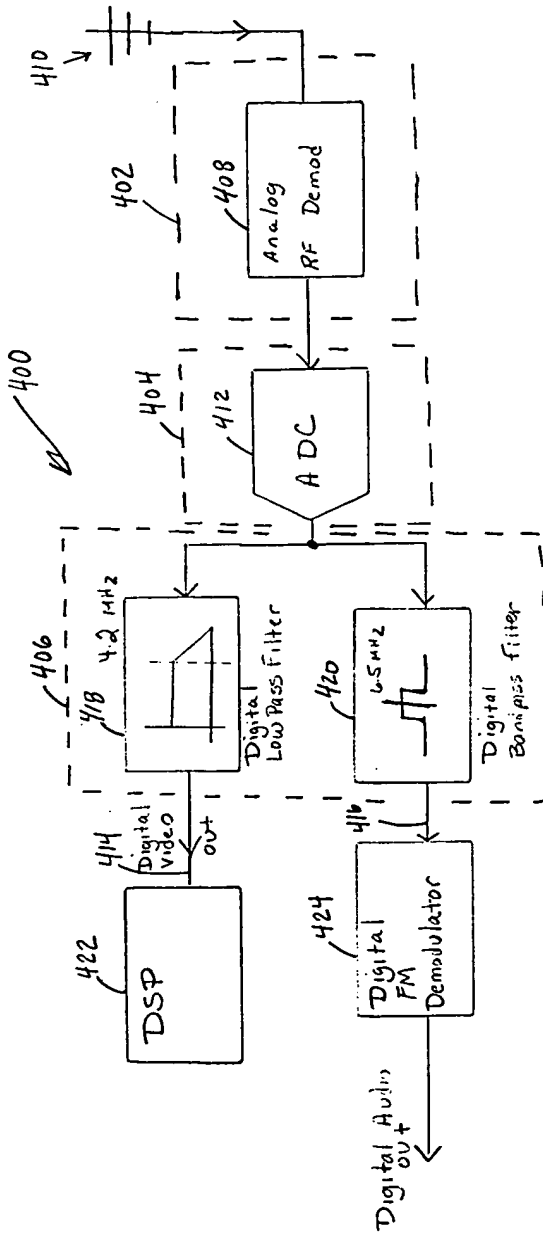


Fig. 13

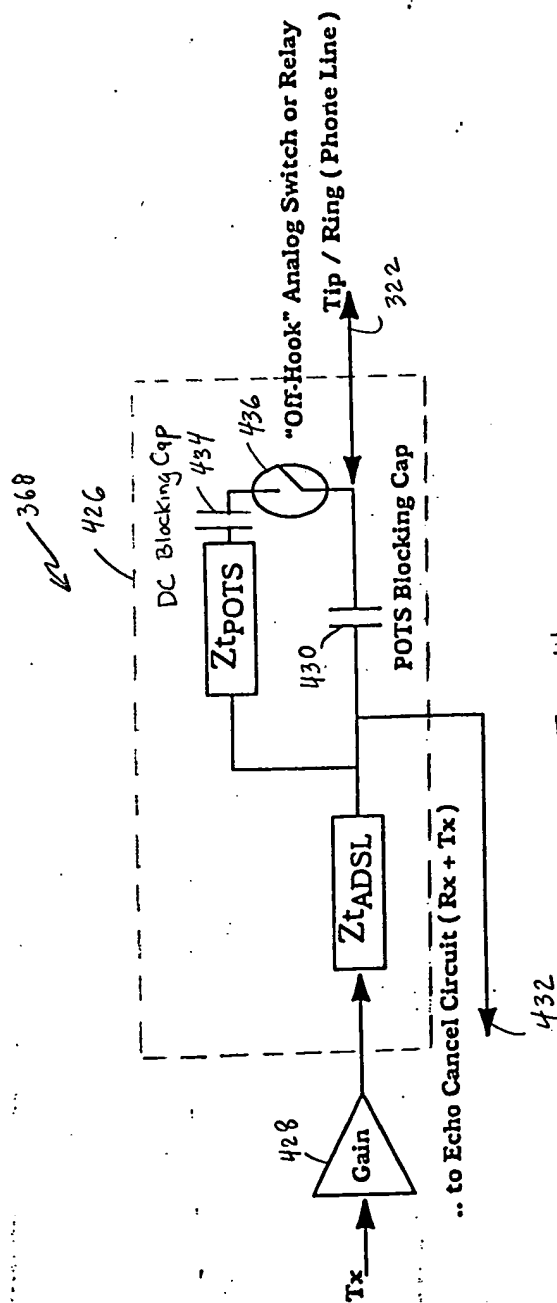


Fig. 14a

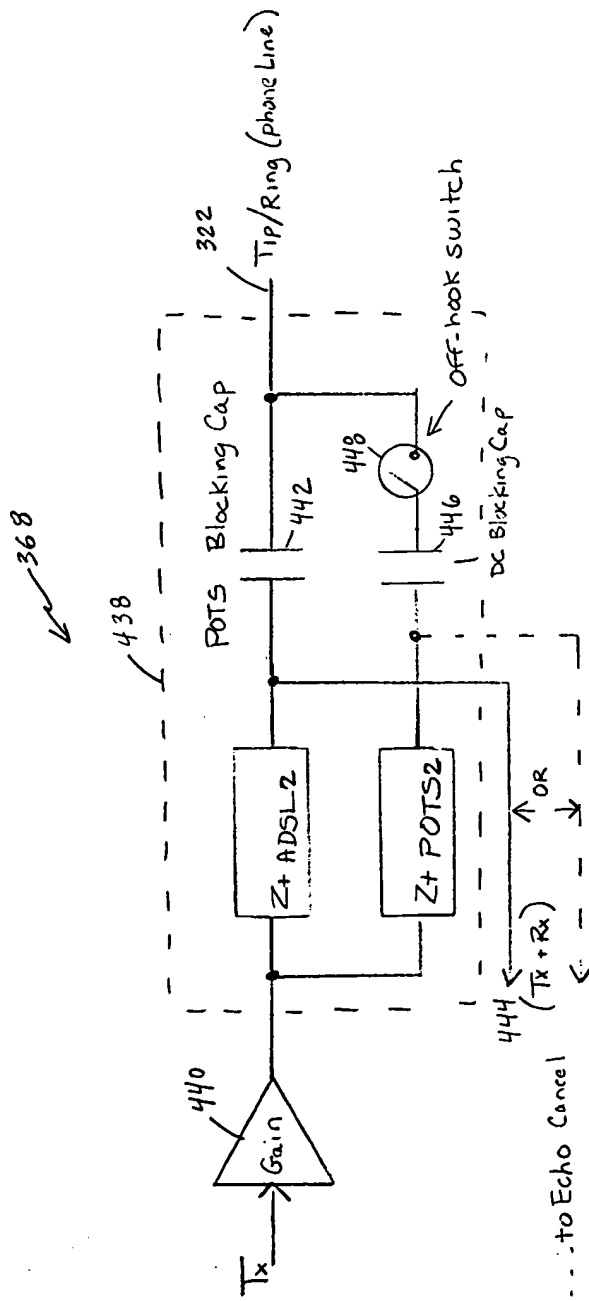


Fig 14b

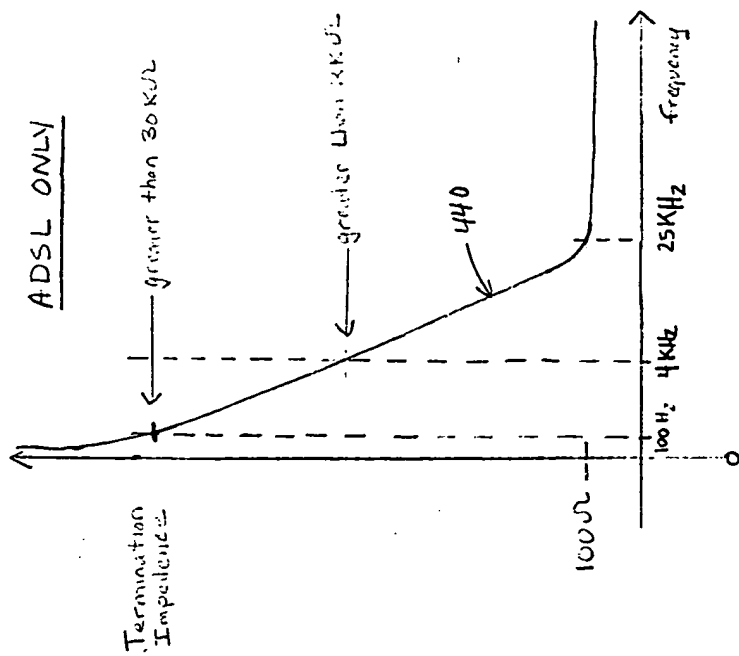


Fig 15a

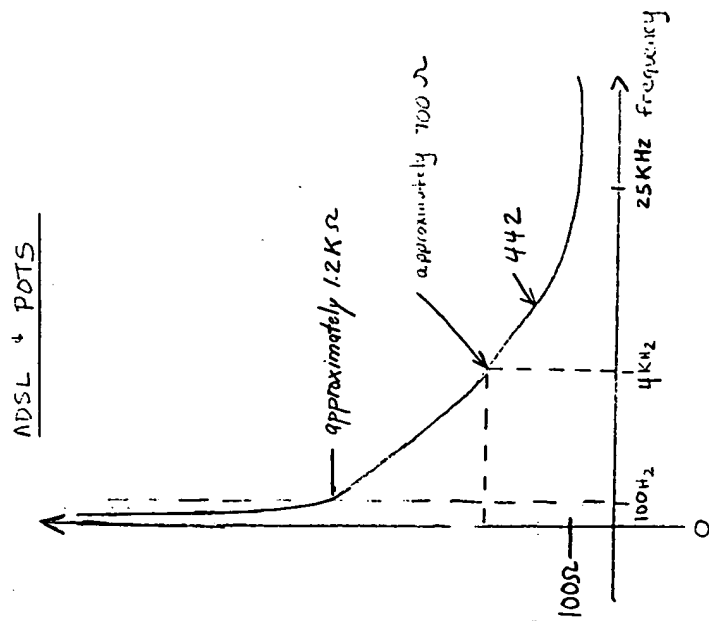


Fig. 15b



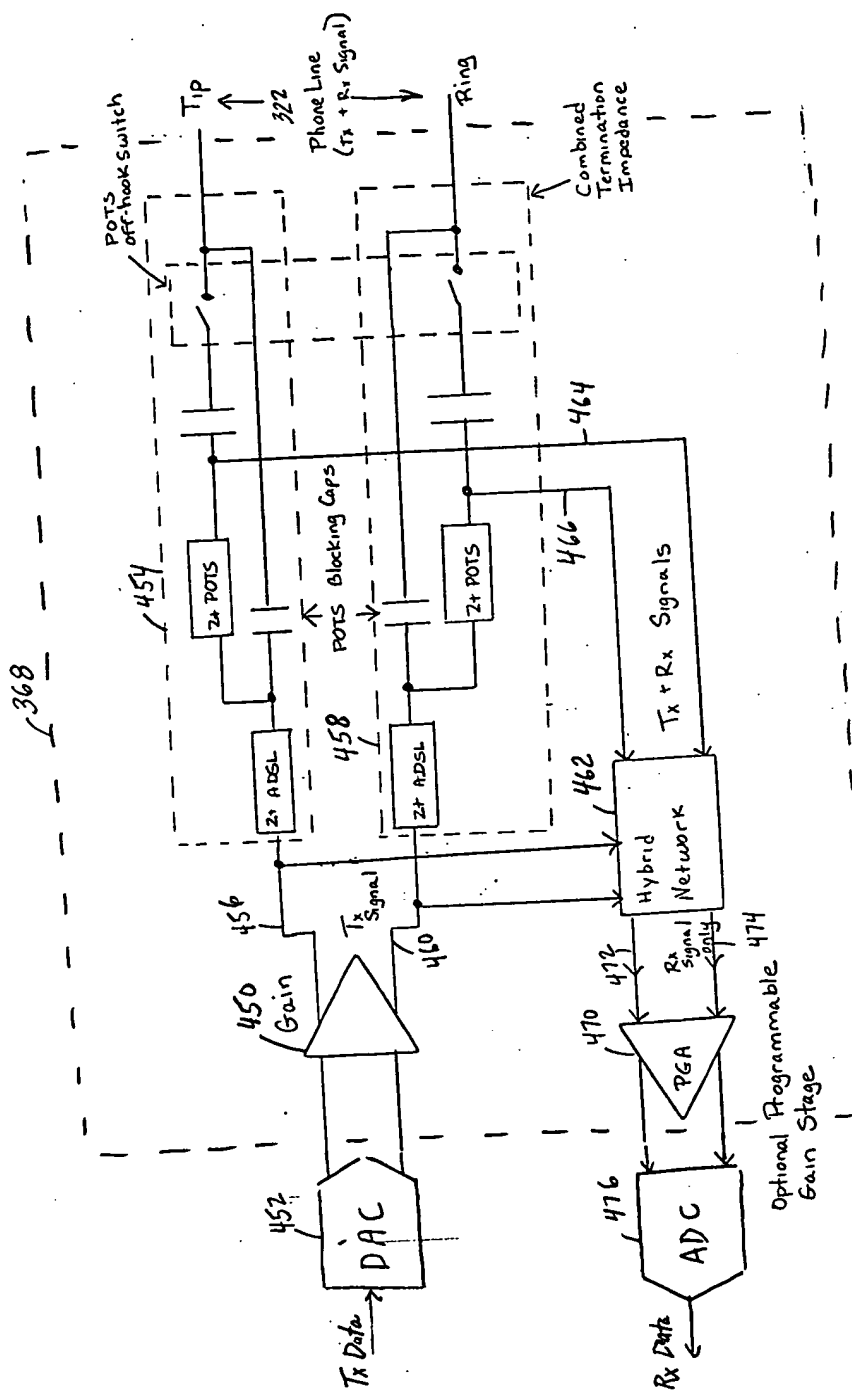
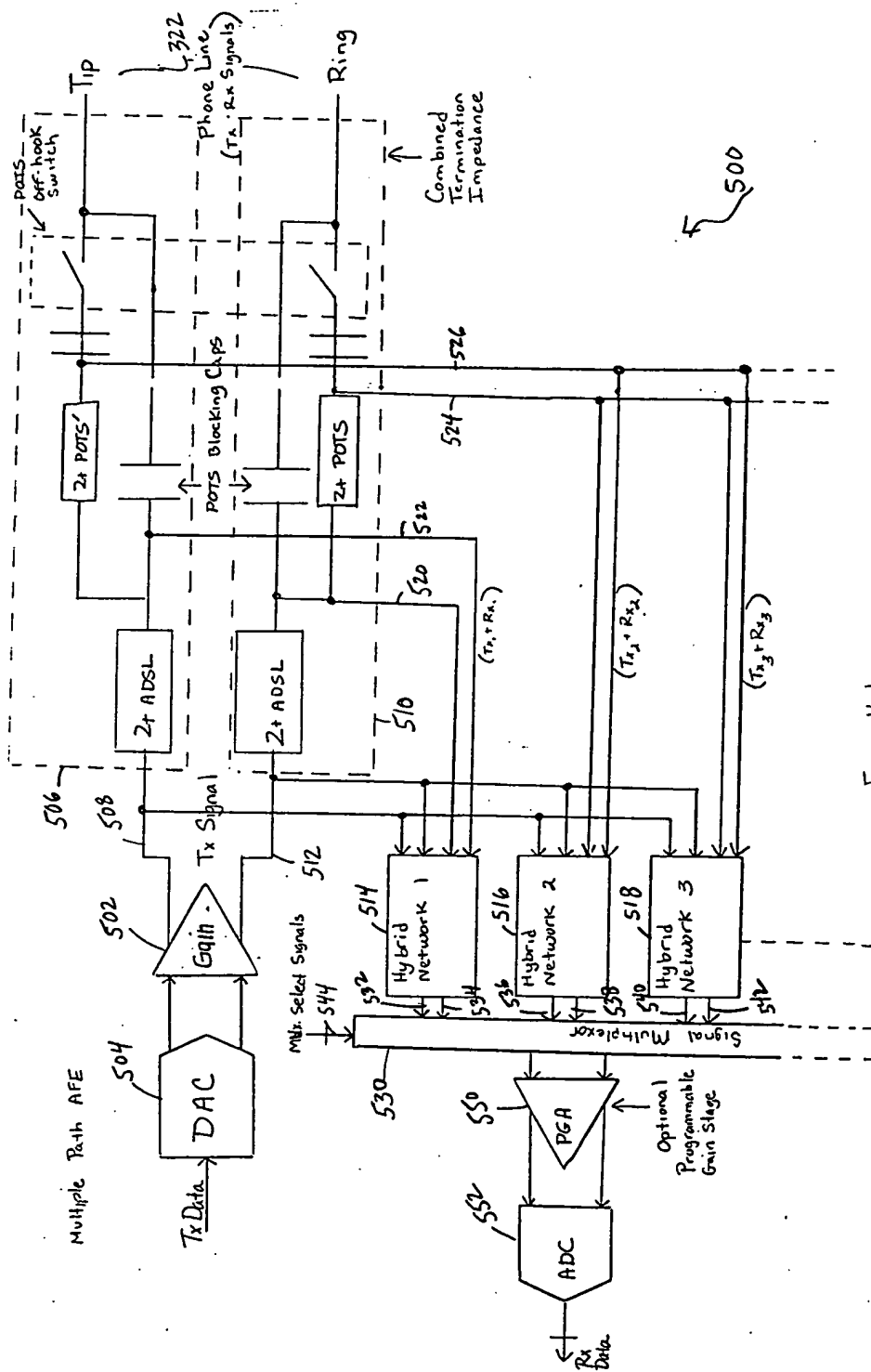


Fig 16a



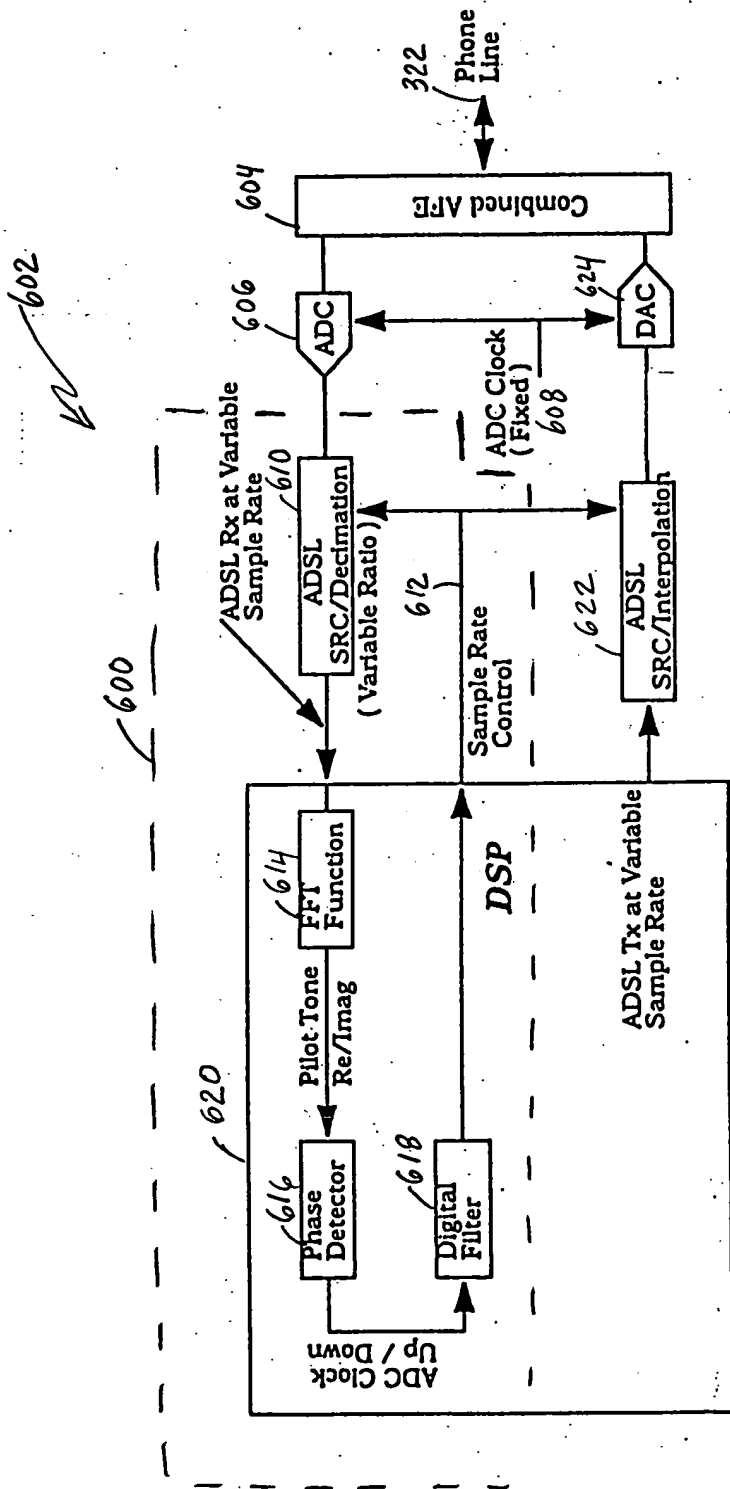


Fig. 17

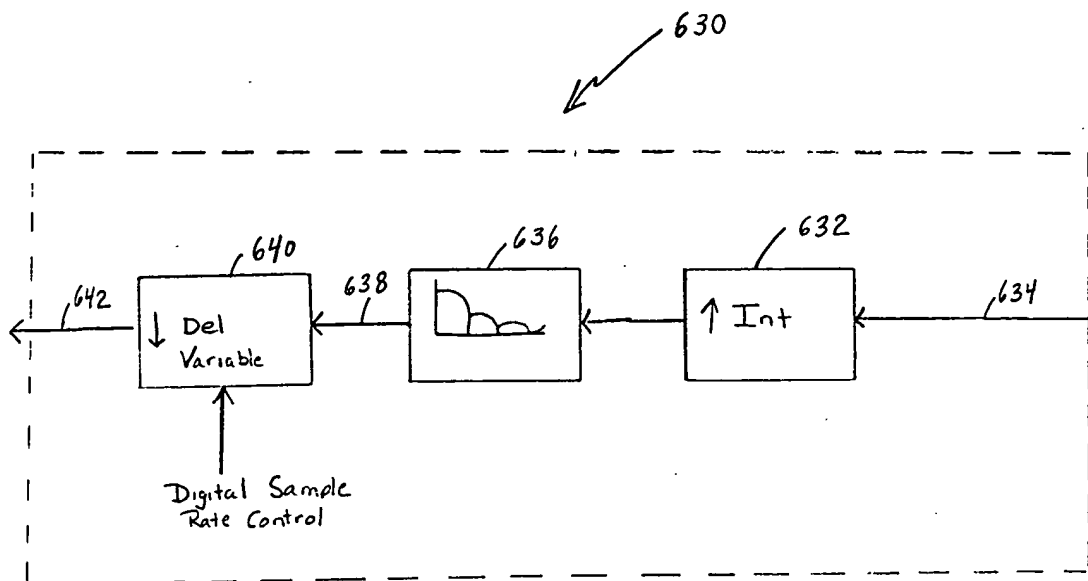


Fig 18

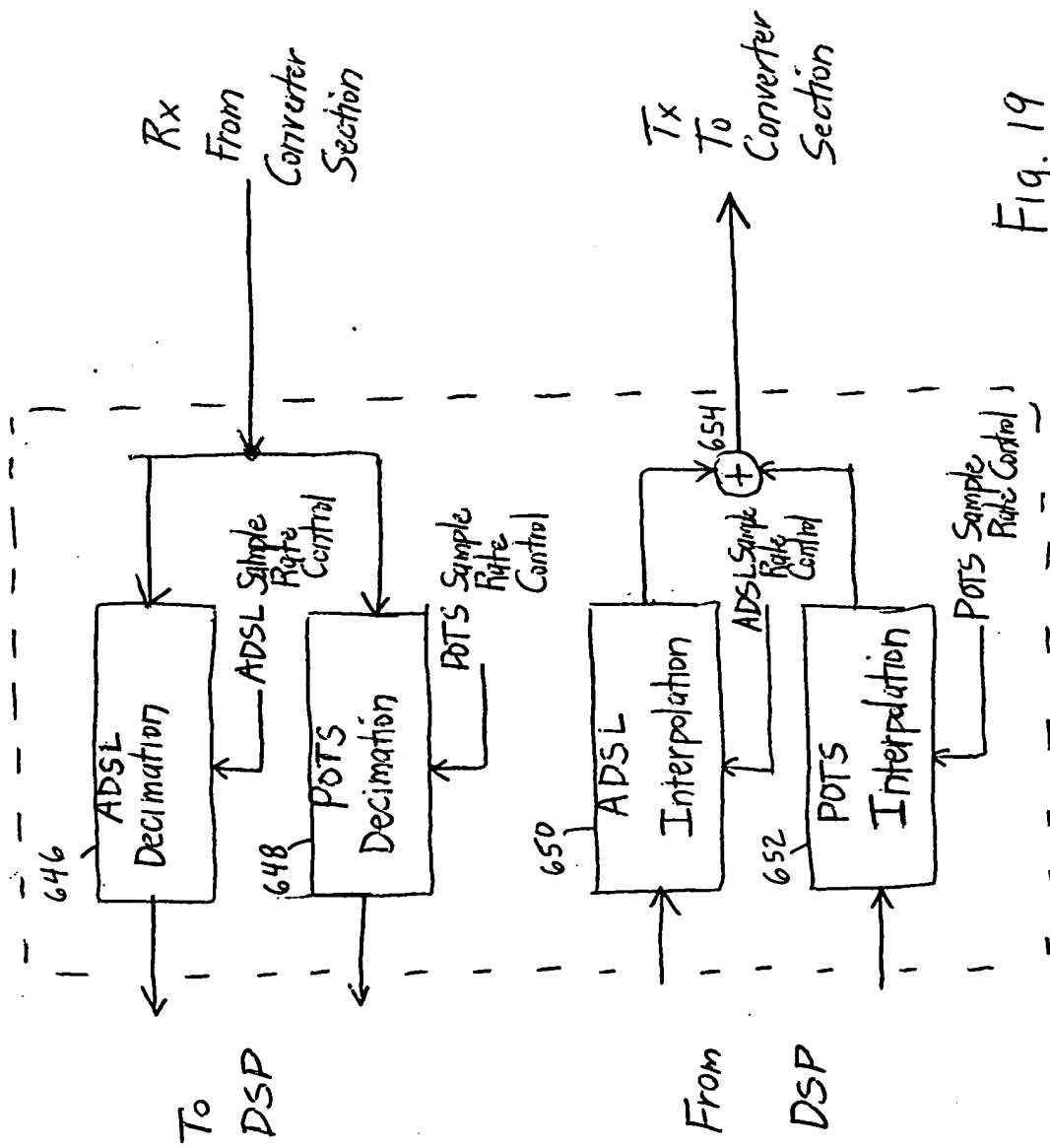
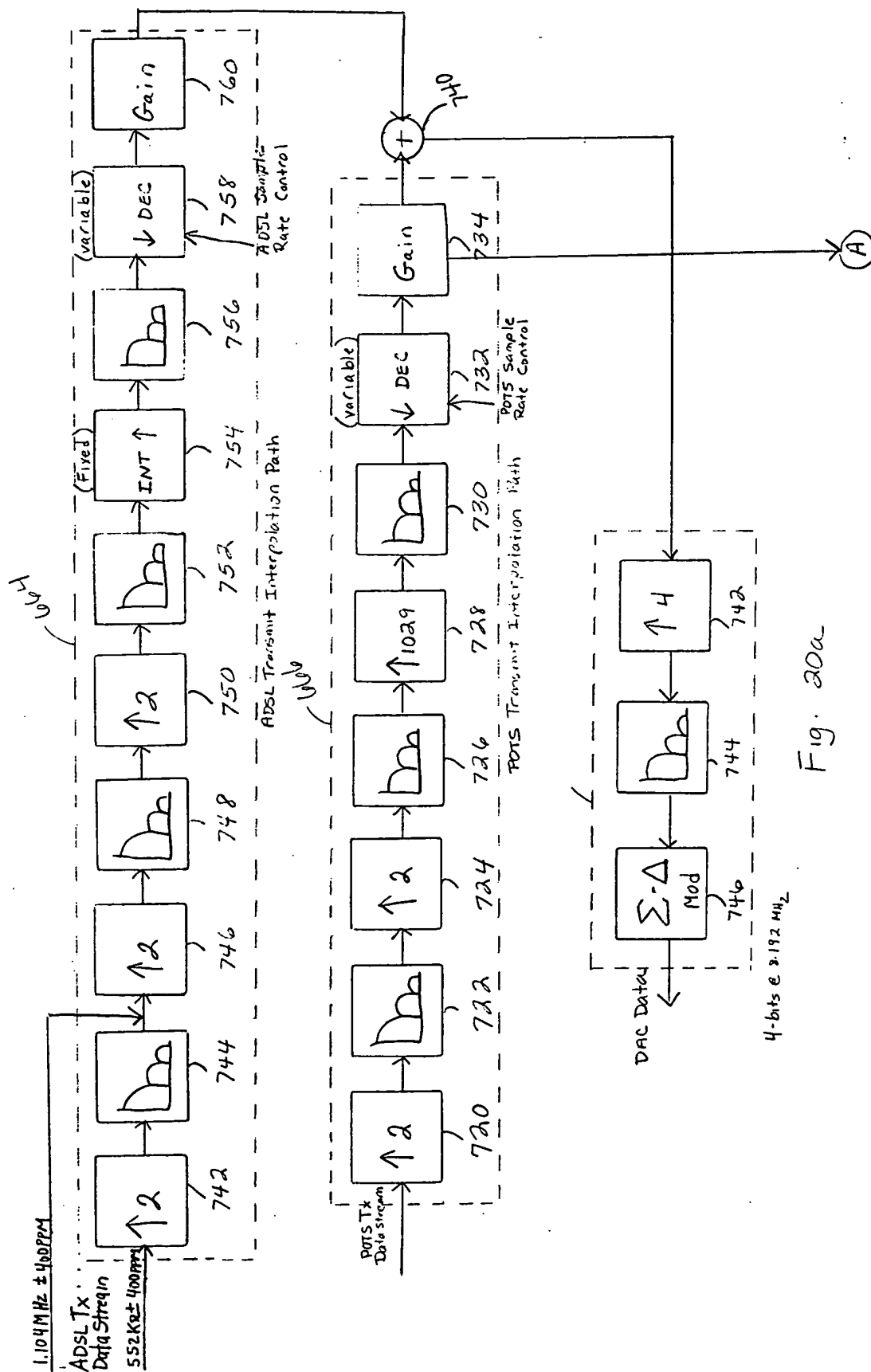


Fig. 19



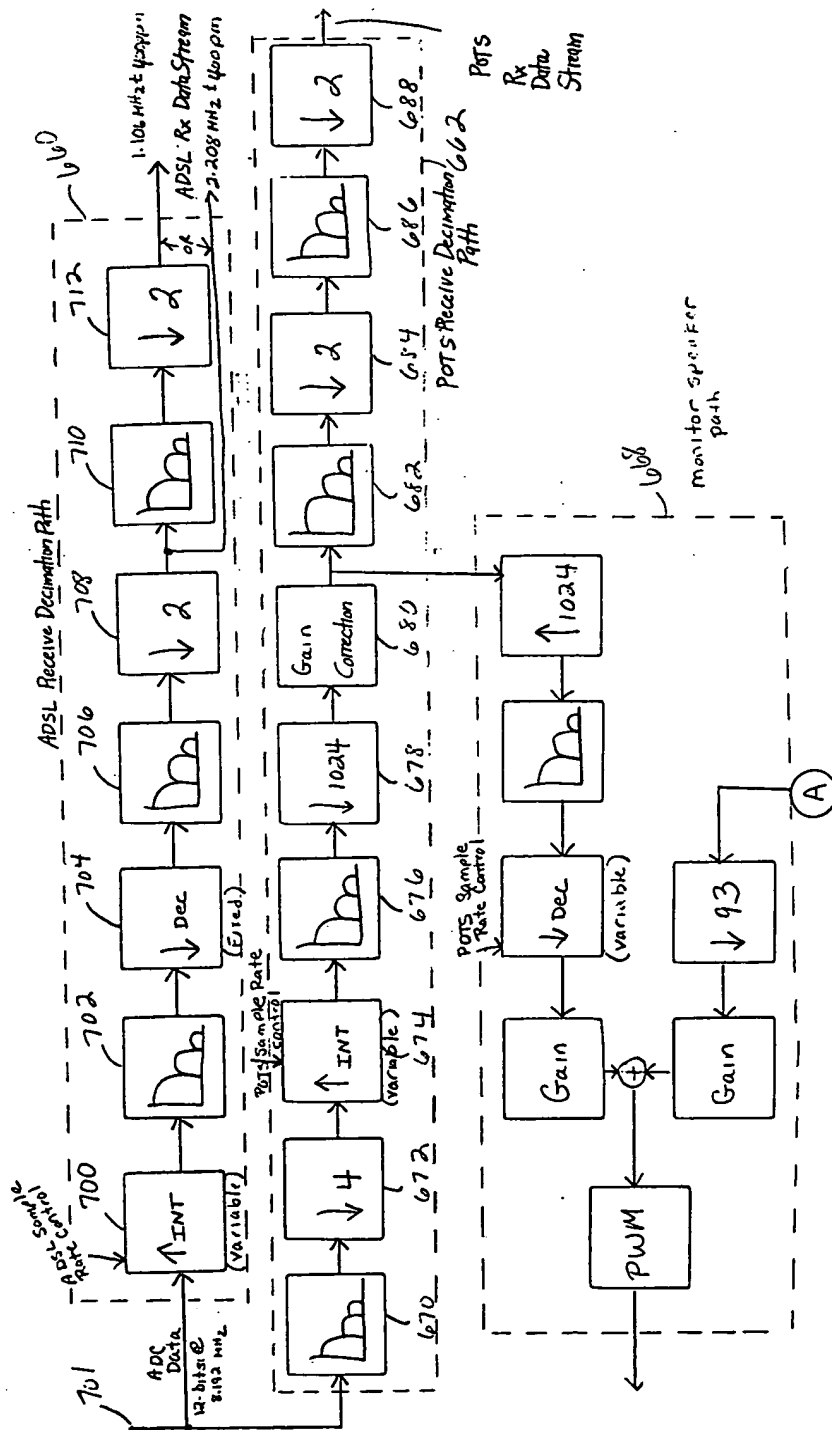
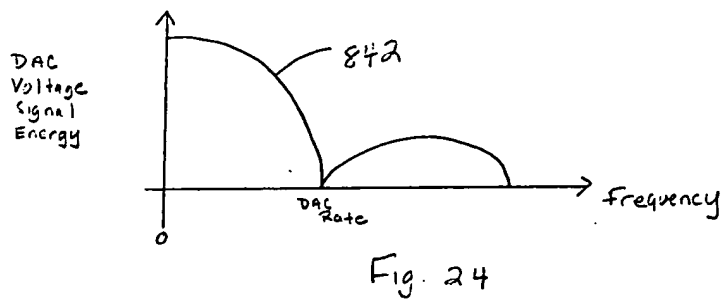
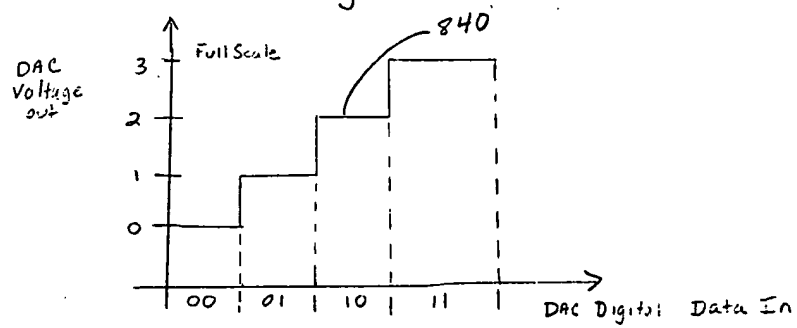
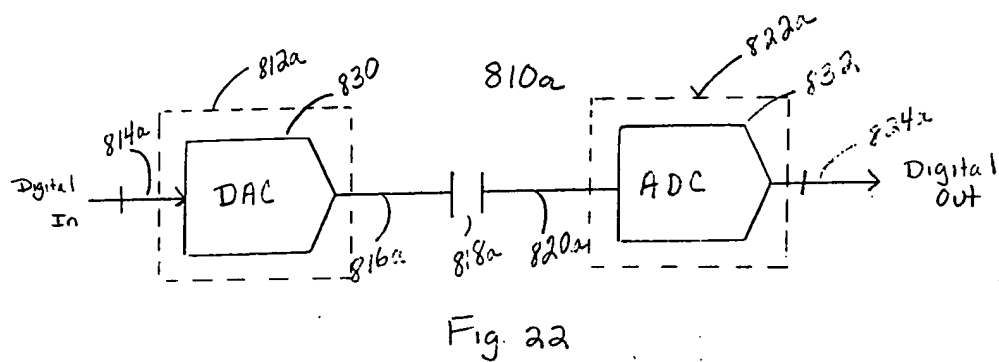
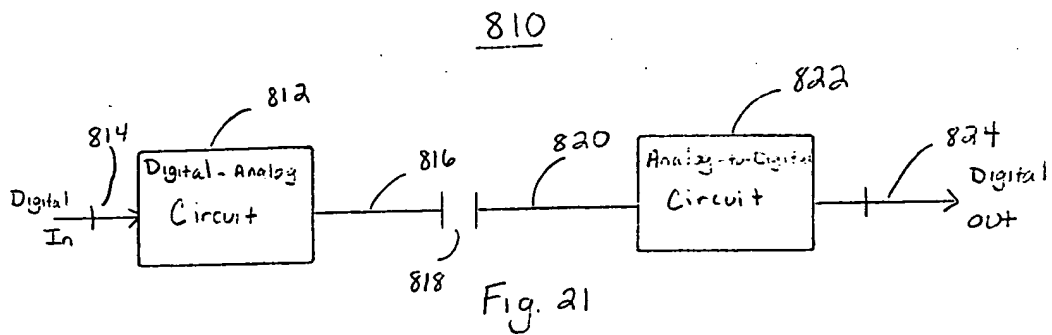


Fig 20b





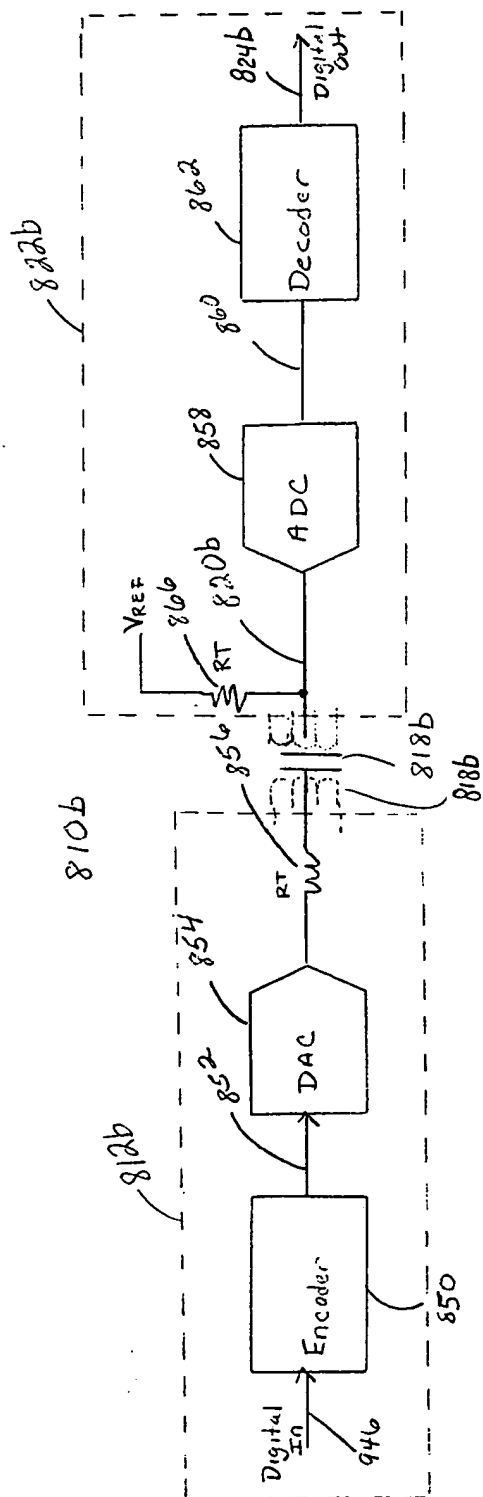


Fig. 25

# ENCODER

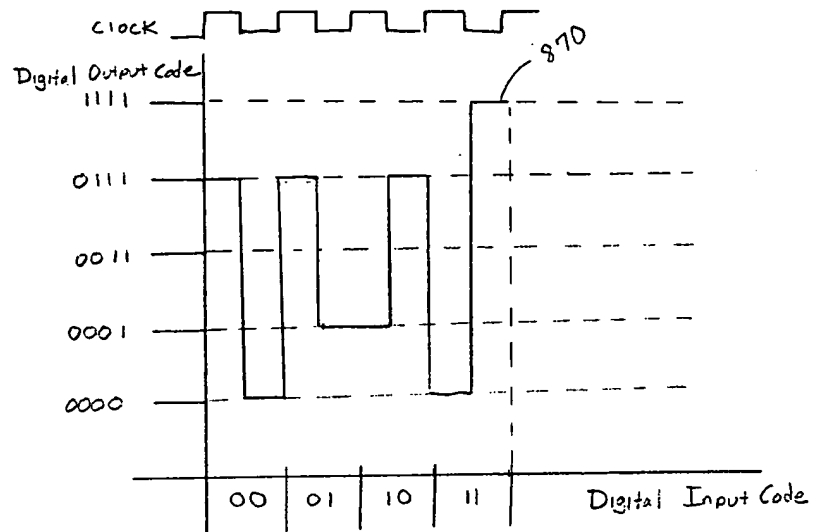


Fig 26

DAC

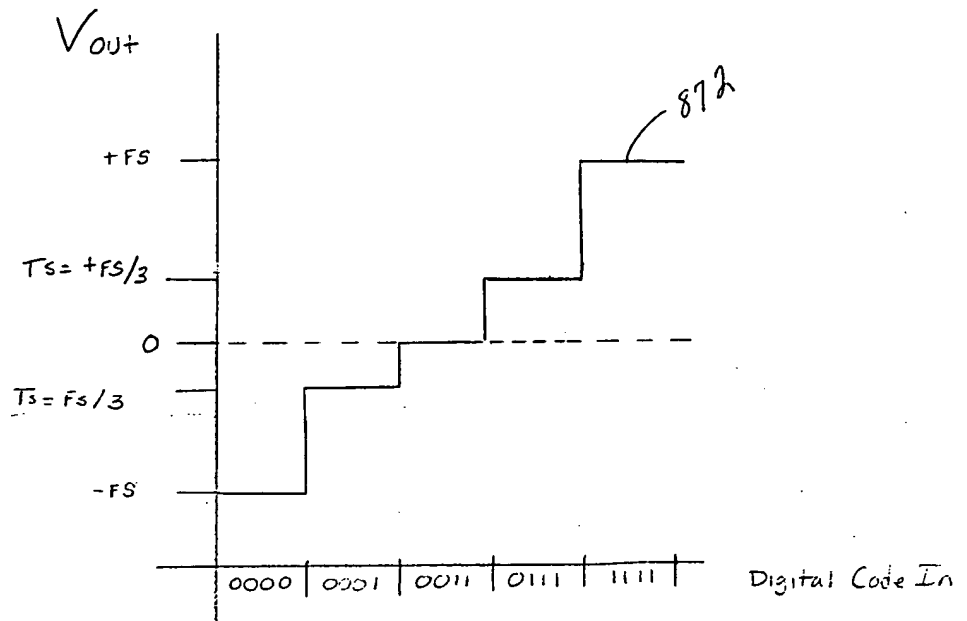


Fig. 27

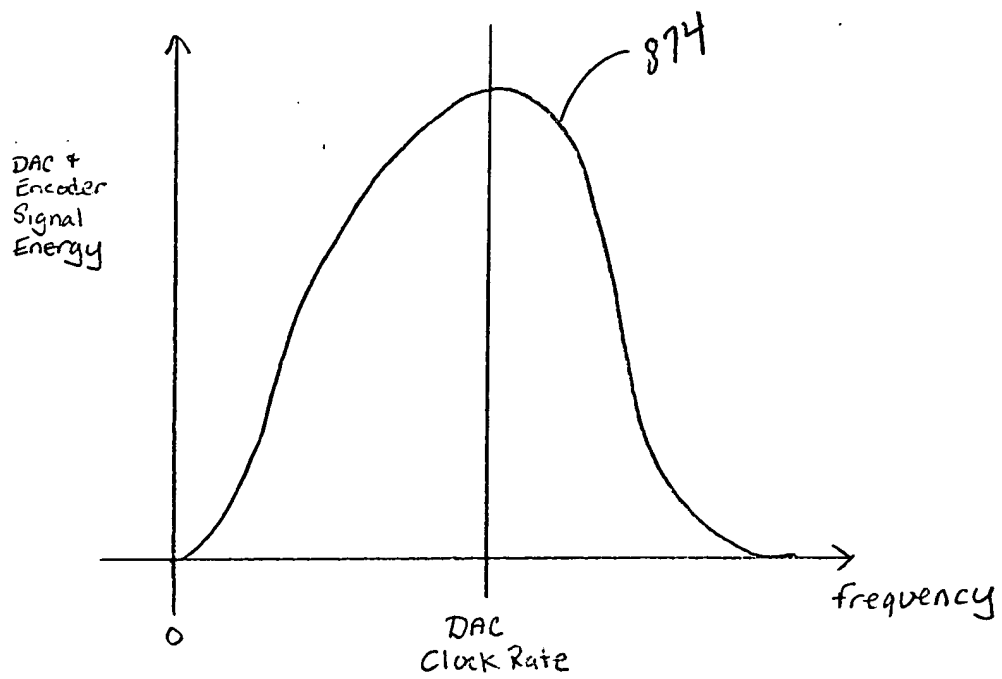
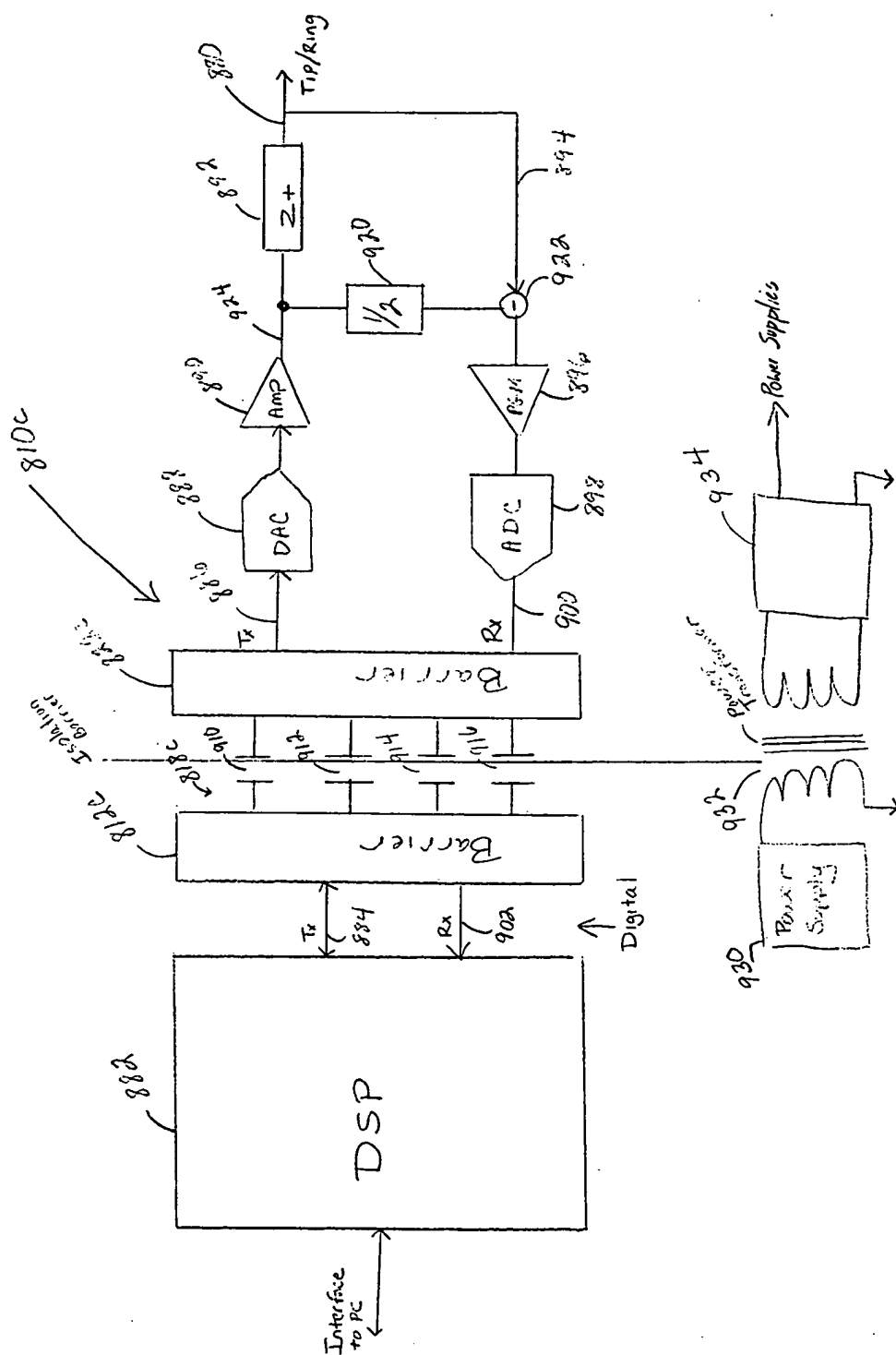
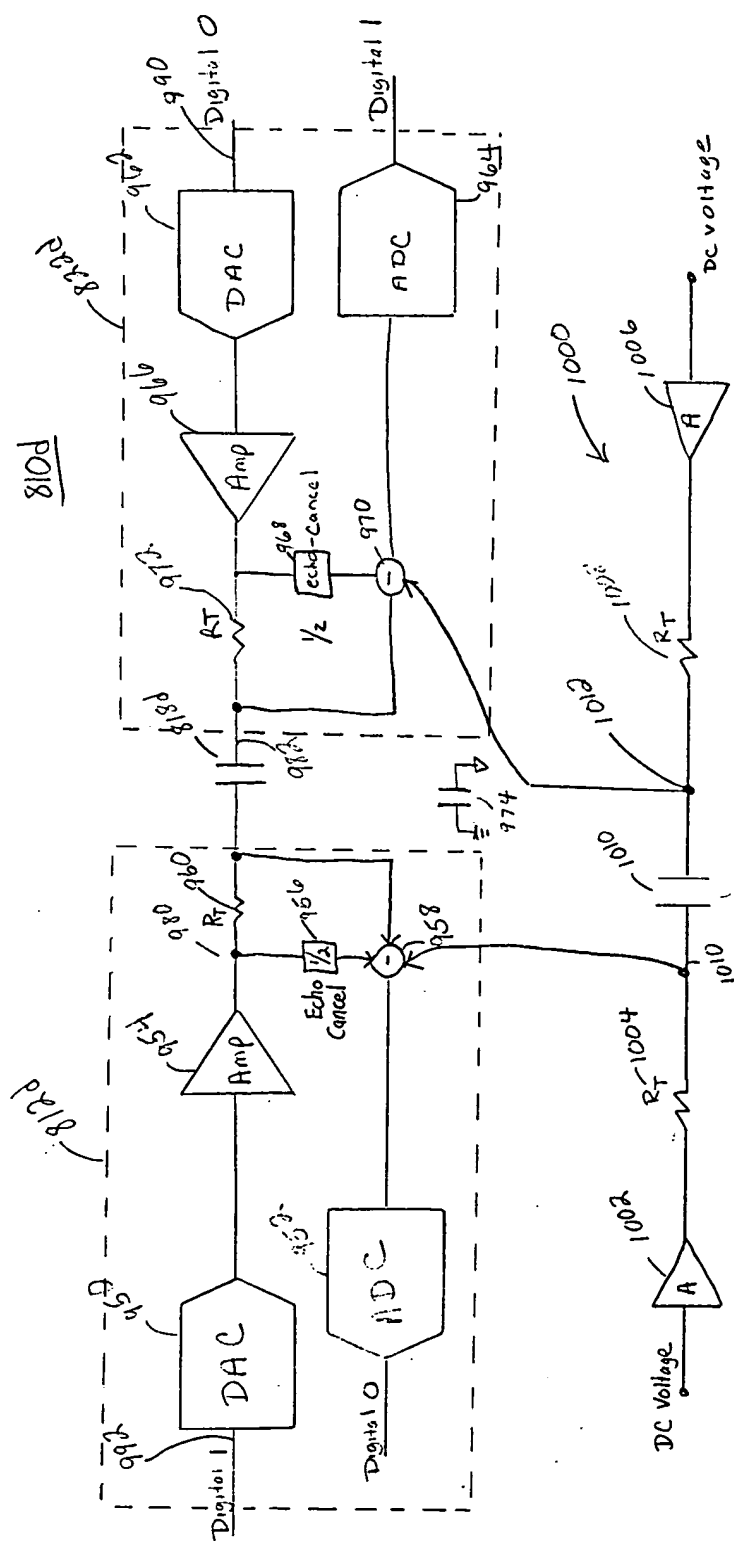


Fig. 28



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# Full Barrier System

810e

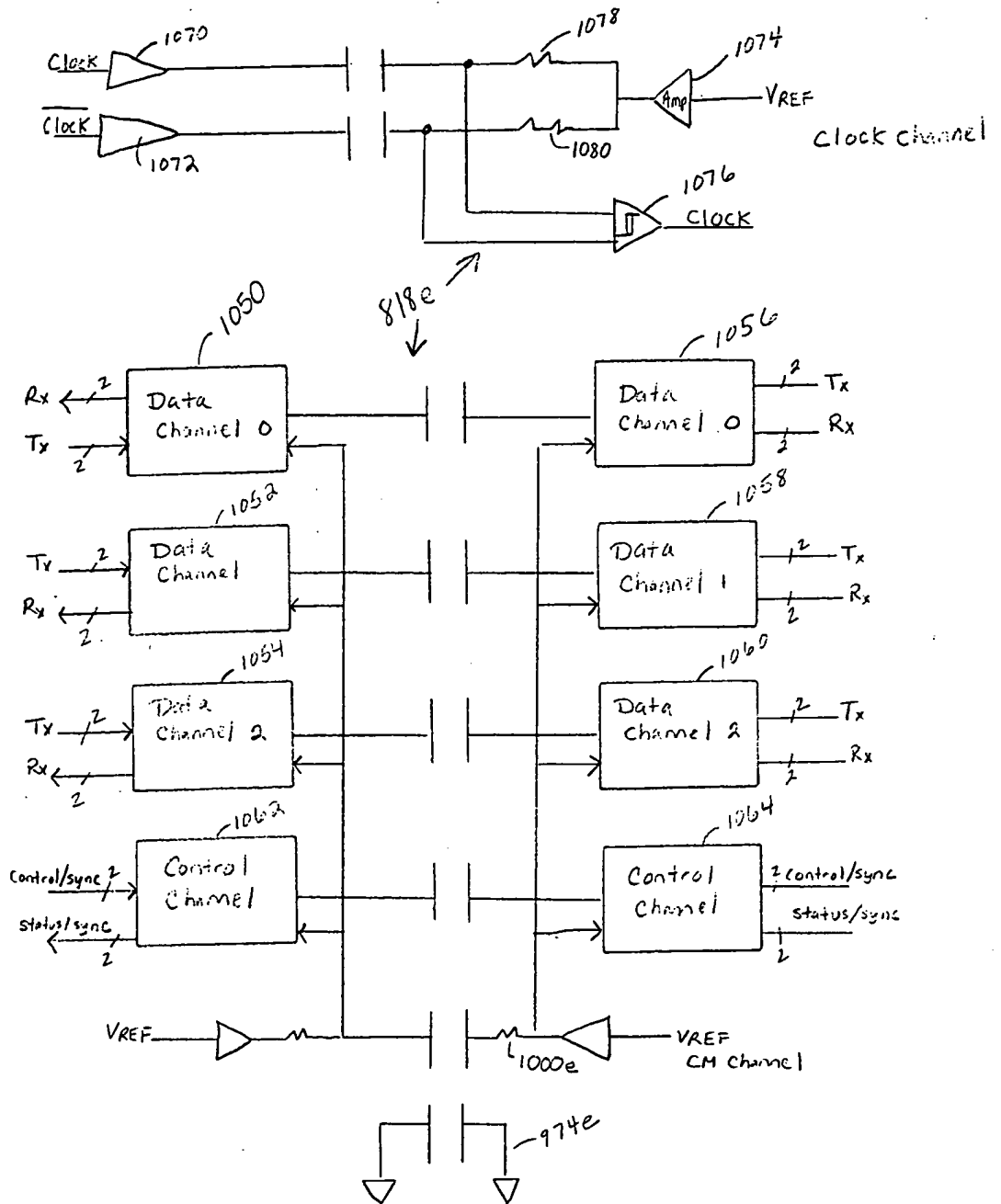


Fig. 31

FIG. 32

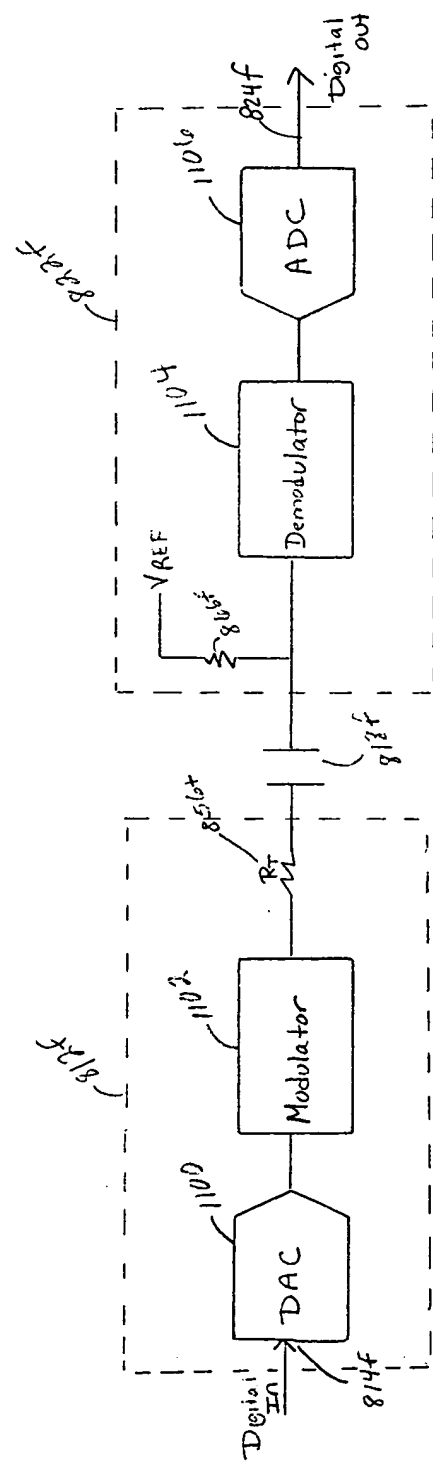


Fig. 32